

1c996 U.S. PTO

10/029571



12/20/01

PATENT NUMBER and  
ISSUE DATE

## U.S. UTILITY Patent Application

APPL NUM 10029571	FILING DATE 12/20/2001	CLASS 702	SUBCLASS 119	GAU 2857	EXAMINER TSA
<b>**APPLICANTS:</b> Takahashi Eiji; Fukumoto Yukihiro; Saito Yoshiyuki; Shibata Osamu; Tanimoto Shinichi; Nakayama Takeshi;					
<b>**CONTINUING DATA VERIFIED:</b>					
<b>BEST AVAILABLE COPY</b>					
<b>** FOREIGN APPLICATIONS VERIFIED:</b> JAPAN 2001-002179 01/10/2001					
PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO			
35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		NAK1-BQ83			
Verified and Acknowledged Examiners's initials					
TITLE : Multilayer board in which wiring of signal line that requires tamper-resistance is covered by component or foil, design apparatus, method, and program for the multilayer board, and mediu					
U.S. DEPT. OF COMM./PAT. & TM-PTO-436L/Rev. 12-94					

<b>NOTICE OF ALLOWANCE MAILED</b>		<b>CLAIMS ALLOWED</b>	
		Assistant Examiner	
<b>ISSUE FEE</b>		<b>DRAWING</b>	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.
		Print Fig.	
		Application Examiner	
<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>		<b>PREPARED FOR ISSUE</b>	
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